REMARKS

The application as originally filed contained claims 1-34, all of which were rejected. In Applicants' previous response mailed June 12, 2001, claims 14 and 15 were removed from examination due to a restriction requirement. These two claims are being reinstated in the present response with Examiner's permission indicated in the present Office Action mailed August 28, 2001. Claims 1, 14, 15, 16, 23, and 30 are being amended, and claims 2-13, 17-22, 24-29, and 31-34 remain unchanged. Accordingly, claims 1-34 are pending in the present application. Applicants submit that no new matter has been added by these amendments. In view of the forgoing amendments and the following remarks, Applicants respectfully request reconsideration of the present application.

Withdraw of Restriction Requirement

Claims 1-34 were presented in the application as originally filed on January 22, 1999. In the previous Office Action mailed May 15, 2001, the Examiner required restriction of prosecution to two of the three Groups, Groups I, II and III. In Applicants' previous response mailed June 12, 2001, Applicants removed claims 14 and 15 from examination. In the present Office Action, the Examiner withdrew the restriction requirement indicating that "claims 14-15 can be added as new claims if Applicant still wishes to retain them." In response, Applicants are reinstating claims 14 and 15.

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Rejection under 35 U.S.C. §102 over Goettsch

In paragraph 3 of the Office Action, the Examiner rejected claims 1-2, 23, and 30 under 35 U.S.C. §102(e) as being anticipated by Goettsch (U.S. Patent No. 6,112,262). Specifically, the Examiner rejected claims 1 and 2 stating that "Goettsch teaches a method for providing ordered data to a device [120, Fig. 1B] over a bus [135 Fig. 1B], the bus providing a communication path for data and associated addresses." Applicants respectfully submit that claims 1 and 2, as amended, overcome this rejection.

Conventionally, the existing art utilizes write combining technology or encoded commands to increase bandwidth for a bus between a dedicated CPU and a graphics device. However, the use of both write combining technology and encoded commands is problematic because write combining technology requires that information be transmitted in an order possibly different than that otherwise expected by a sender. The use of encoded commands, on the other hand, requires that received parameters be in a predefined order with respect to a command. (See background of the present Specification).

The claimed invention provides methods and systems to overcome the obstacles of both write combining technology and encoded commands. In a broad aspect, the claimed invention ***reorders items of data***, which are out of a predefined order due to data transmission from a data source to a data destination, ***by utilizing address information in the data source***. Specifically, claim 1, as amended, recites a method of providing ordered data transmitted from a data source to a data destination over a bus. The method of claim 1 comprises the steps of:

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writing items of data into sequentially ordered areas of a memory, the items of data having a predefined order in the data source, the sequentially ordered areas of memory being identifiable by addresses, each item of data being placed in an area ***having an associated address in the data source***;

transmitting the items of data and associated addresses from the data source to the data destination over the bus, the items of data being ***transmitted in an order other than the predefined order***;

receiving the items of data and ***the associated addresses in the data source*** from the bus;

examining the ***associated address in the data source*** for each item of data received from the bus; and

placing each item of data received from the bus in one of multiple sequentially arranged areas of a storing buffer, each item being placed ***based on the associated address in the data source*** for each item, the placement of the items of data causing reordering of the received items of data. (Emphasis added)

Support of the amendments to claim 1 is found in the present Specification, at page 4, lines 4-19; at page 7, lines 4-25; and at page 19, lines 5-12.

In contrast, Goettsch does not disclose or suggest a step of "examining the ***associated address in the data source*** for each item of data" or "placing items of data in a storing buffer ***based on the associated addresses in a data source***." Rather, Goettsch discloses transmitting addresses that indicate the memory locations where transmitted data items are to be stored by a co-processor 120 (see Fig. 1B; abstract; and column 6, line 56 – column 7, line 11 of Goettsch's Specification). Stated differently, in Goettsch, the transmitted addresses are utilized to indicate ***memory locations in a data destination***; these transmitted addresses are not utilized to indicate associated addresses ***in a data source*** for items of data. Therefore, claim 1, as amended, is allowable under 35 U.S.C. §102(e) over Goettsch. Claim 2 depends from claim 1 and is therefore allowable for at least the same reasons as claim 1.

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In paragraph 5, the Examiner rejected independent claim 23. Applicants respectively submit that claim 23, as amended, overcomes this §102 rejection. Specifically, claim 23, as amended, recites a computer device for reordering incoming data received from a data source over a bus interface, wherein the incoming data has a predefined order and ***associated address information in the data source***. The computer device of claim 23 comprises:

> a receive buffer which receives the incoming data and the associated address information ***in the data source***, the received incoming data being out of the predefined order;
>
> a storage buffer which stores the incoming data in an order ***based on the associated address information in the data source***; and
>
> a detector which determines proper placement of the out order incoming data in the receive buffer in the storage buffer ***based on the associated address information in the data source***. (Emphasis added).

In contrast, Goettsch does not disclose or suggest "a storage buffer which stores the incoming data ***in an order based on the associated address information in the data source***" or "a detector which determines proper placement of the out order incoming data in the receive buffer in the storage buffer ***based on the associated address information in the data source***" as is required in claim 23. Therefore, claim 23, as amended, is allowable under 35 U.S.C. §102(e) over Goettsch.

In paragraph 6, the Examiner rejected independent claim 30 as being anticipated by Goettsch. Applicants submit that claim 30, as amended, overcomes this rejection. Specifically, claim 30, as amended, recites a method for reordering incoming data transmitted from a data source to a data destination. The method of claim 30 comprises the steps of:

> receiving at the data destination the incoming data and the address information transmitted from the data source;

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arranging, in the predefined order, the incoming data ***based on the address information in the data source contained*** within the incoming data; and

storing the arranged data temporarily. (Emphasis added).

In contrast, Goettsch does not disclose or suggest a step of "arranging, in the predefined order, the incoming data ***based on the address information in the data source*** ..." Therefore, claim 30, as amended, is allowable under 35 U.S.C. §102(e) over Goettsch.

Rejection under 35 U.S.C. §102 over Palanca

In paragraph 7, the Examiner rejected claims 23-25 and 30-34 under 35 U.S.C. §102(e) as being anticipated by Palanca et al. (US Patent Number 6,122,715). Further in paragraph 8, the Examiner particularly rejected independent claim 23. Applicants respectively traverse this rejection. Specifically, claim 23, as amended, recites a computer device comprising in part:

a storage buffer which stores the incoming data in an order ***based on the associated address information in the data source***; and

a detector which determines proper placement of the out order incoming data in the receive buffer in the storage buffer ***based on the associated address information in the data source***. (Emphasis added).

In contrast, Palanca et al. does not disclose or suggest "a storage buffer which stores the incoming data in an order ***based on the associated address information in the data source***" or "a detector which determines proper placement ... ***based on the associated address information in the data source***." Rather, Palanca et al. utilizes a WC pointer to locate a buffer to be operated on (see Palanca's Specification, Fig. 7 and Fig. 8; column 10, lines 19-65; and column 11, lines 1-25). In other words, Palanca et al. stores

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incoming data in an order indicated by the WC pointer, but ***not*** in an order indicated by the ***address information in a data source***. Therefore, claim 23 is allowable under 35 U.S.C. §102(e) over Palanca et al.

In paragraph 9, the Examiner rejected claims 24-25. Applicants respectfully submit that claims 24-25 depend from independent claim 23 and are therefore allowable for at least the same reasons as claim 23.

In paragraph 10, the Examiner rejected independent claim 30. Applicants respectfully traverse this rejection. Specifically, claim 30, as amended, recites a method comprising, in part, a step of:

> arranging, in the predefined order, the incoming data ***based on the address information in the data source*** contained within the incoming data; ... (Emphasis added).

In contrast, Palanca et al. does not disclose or suggest a step of "arranging, in the predefined order, the incoming data ***based on the address information in the data source***." Therefore, claim 30 is allowable under 35 U.S.C. §102(e) over Palanca et al.

In paragraph 11, the Examiner rejected claims 31-34. Applicants respectfully submit that claims 31-34 depend from independent claim 30 and are therefore allowable for at least the same reasons as claim 30.

Rejection under 35 U.S.C. §103 over Goettsch

In paragraph 13, the Examiner rejected claims 3-9, 14-15, 24-29, and 31-34 under 35 U.S.C. 103(a) as being unpatentable over Goettsch.

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In paragraphs 14-17, the Examiner particularly rejected claims 3-9, all of which depend from claim 1. As discussed above, amended claim 1 recites a method comprising, in part, a step of:

> placing each item of data received from the bus in one of multiple sequentially arranged areas of a storing buffer, each item being placed ***based on the associated address in the data source*** for each item, ... (Emphasis added).

In contrast, Goettsch does not disclose or suggest a step of "placing each item ***based on the associated address in the data source*** for each item." Therefore, claim 1 is allowable under 35 U.S.C. §103(a) over Goettsch. Because claims 3-9 depend from claim 1, they are allowable for at least the same reasons as claim 1.

In paragraph 18, the Examiner rejected claims 14-15 over Goettsch. Applicants respectfully submit that independent claim 14, which is being reinstated and amended, overcomes this rejection. Specifically, claim 14 recites a method of increasing effective bus bandwidth for transmitting items of data from a data source to a data destination. The method of claim 14 comprises the steps of:

> defining a region of a memory as a write combining memory type, the region of the memory being comprised of addressable locations of processor memory, the addressable locations identifiable by ***addresses in the data source***;
>
> writing items of data into the region in a sequential order of the addressable locations, the items of data comprising encoded commands and parameters associated with the encoded commands, ***the items of data having a predefined order in the data source***;
>
> transmitting the items of data and addresses of the items of data from the data source to the data destination over a bus, the items of data being transmitted ***in an order other than the predefined order***; and
>
> arranging the transmitted items of data in an order ***corresponding to the addresses in the data source*** for the items of data to reorder the transmitted items of data. (Emphasis added).

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In contrast, Goettsch does not disclose or suggest a step of "arranging the transmitted items of data in an order ***corresponding to the addresses in the data source***" as is required by claim 14. Therefore, claim 14 is allowable under 35 U.S.C. §103(a) over Goettsch. Because claim 15, which is being reinstated and amended, depends from independent claim 14, claim 15 is allowable for at least the same reasons as claim 14.

In paragraphs 19-22, the Examiner rejected claims 24-29, all of which depend from independent claim 23. As discussed above, Goettsch does not disclose or suggest "a storage buffer which stores the incoming data ***in an order based on the associated address information in the data source***" or "a detector which determines proper placement of the out order incoming data ... ***based on the associated address information in the data source***" as is required by independent claim 23. Therefore, claim 23 is allowable under 35 U.S.C. §103(a) over Goettsch. Because claims 24-29 depend from independent claim 23, they are allowable for at least the same reasons as claim 23.

In paragraph 20, the Examiner particularly rejected claim 26 stating that "[i]t was further well known in the art that graphics memory was able to store blocks of data retrieved from a storage buffer" by referencing to Glew et al. (U.S. Patent Number 5,561,780). Applicants respectfully submit that neither Goettsch, nor Glew et al., nor any combination thereof, disclose or suggest "a storage buffer which stores the incoming data ***in an order based on the associated address information in the data source***" or "a detector which determines proper placement of the out order incoming data ... ***based on the associated address information in the data source***" as is required by claims 24-29.

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In paragraph 23, the Examiner rejected claims 31-34. As discussed above, Goettsch does not disclose or suggest a step of "arranging, in the predefined order, the incoming data ***based on the address information in the data source***" as is required by independent claim 30. Therefore, independent claim 30 is allowable under 35 U.S.C. §103(a) over Goettsch. Because claims 31-34 depend from claim 30, they are allowable for at least the same reasons as claim 30.

Rejection under 35 U.S.C. §103 over Palanca

In paragraph 24, the Examiner rejected claims 1-9, 16-17, and 25-29 under 35 U.S.C. 103(a) as being unpatentable over Palanca et al.

In paragraph 25, the Examiner particularly rejected claim 1 stating that "Palanca et al. teaches a method for providing ordered data to a device." The Examiner conceded that "Palanca et al. does not specifically teach placing each item of data in one of the multiple sequentially arranged areas of a storing buffer." However, the Examiner went on to assert that:

> ... It is, however, well known in the art at the time the invention was made for placing data items from write combine buffers in one of the multiple sequentially arranged areas of a frame buffer before display (see Glew, U.S. Pat. No. 5,561,780 to same assignee as Palanca's: col. 11, lines 44-57).

Applicants respectfully submit that claim 1, as amended, overcomes this rejection. Specifically, claim 1, as amended, recites a method comprising, in part, steps of:

> examining the ***associated address in the data source*** for each item of data ...; and
>
> placing each item of data received from the bus in one of multiple sequentially arranged areas of a storing buffer, each item being placed

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based on the associated address in the data source for each item, ... (Emphasis added)

In contrast, neither Palanca et al., nor Glew et al., nor any combination thereof, discloses or suggests a step of "examining the ***associated address in the data source*** for each item of data ..." or "placing each item of data ***based on the associated address in the data source*** for each item." Therefore, claim 1, as amended, is allowable under 35 U.S.C. §103(a) over Palanca et al. or Glew et al.

In paragraphs 26-29, the Examiner rejected claims 2-9. Applicants submit that claims 2-9 depend from claim 1 and are therefore allowable for at least the same reasons as claim 1.

In paragraph 30, the Examiner rejected independent claim 16 in view of Palanca et al. Applicants respectfully submit that claim 16, as amended, overcomes this rejection. Specifically, claim 16, as amended, recites a bus interface bus interface unit of a computer device comprising:

> a plurality of storage buffers each having a plurality of slots for storing data items, the plurality of slots ***being identifiable by addresses in the data source***;
>
> a first router for routing the data items received from the bus to a particular one of the plurality of storage buffers ***based on*** a first part of ***the addresses in the data source*** associated with the data items; and
>
> a plurality of second routers for each of the storage buffers for routing the data items routed to the particular one of the storage buffers to one of the slots in the particular one of the storage buffers ***based on*** a second part of ***the addresses in the data source*** associated with the data items.

In contrast, Palanca et al. does not disclose or suggest "a first router that routers data items to a storage buffers ***based on*** a first part of ***the addresses in a data source***" or "a plurality of second routers that router the data items to the storage buffers ***based on*** a

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second part of ***the address in the data source***." Rather, as discussed above, Palanca et al. utilizes a WC point to locate a buffer to be operated on (see Palanca's Specification, Fig. 7 and Fig. 8; column 10, lines 19-65; and column 11, lines 1-25). Therefore, claim 16 is allowable under 35 U.S.C. 103(a) over Palanca et al. Claim 17 depends from independent claim 16 and is therefore allowable for at least the same reasons as claim 16.

In paragraphs 32-36, the Examiner rejected claims 25-29, all of which depend from independent claim 23. As discussed above, Palanca et al. does not disclose or suggest "a storage buffer which stores the incoming data ***in an order based on the associated address information in the data source***" or "a detector which determines proper placement of the out order incoming data ... ***based on the associated address information in the data source***" as is required by claim 23. Therefore, claim 23, as amended, is allowable under 35 U.S.C. §103(a) over Palanca et al. Because claims 25-29 depend from claim 23, they are allowable for at least the same reasons as claim 23.

In paragraph 34, the Examiner particularly rejected claim 26 stating that "Palanca teaches writing combining buffers." To support the rejection, Examiner asserted that:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made that Palanca teaches a graphics memory connected to the storage buffer and able to store blocks of data retrieved from the storage buffer since it was well known in the art at the time of the invention was made for write combining buffers to store blocks of graphics data for transmission to a graphics memory (see Glew, U.S. Pat. No. 5,561,780 to same assignee as Palanca's: frame buffer 22, Fig. 1).

Applicants respectfully submit that neither Palanca et al., nor Glew et al., nor any combination thereof, discloses or suggests "a first router that routers data items to a storage buffers based on a first part of ***the addresses in the data source***" or "a plurality of

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second routers that router the data items to the storage buffers based on a second part of ***the address in the data source***" as is required in claim 26.

Allowable Subject Matter

In paragraph 37, the Examiner objected to claims 10-13 and 18-22 as being dependent upon a rejected base claim. Applicants note with appreciation that the Examiner indicated that these claims "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." Based on the amendments and remarks submitted in the present response, Applicants respectfully submit that claims 10-13 and 18-22 are allowable.

Conclusion

For the reasons discussed above, Applicants respectfully request withdrawal of the outstanding Objections and Rejections and allowance of the pending claims 1-34.

Respectfully submitted,

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Appendix: Marked-up copy of the amended Claims

1. (once amended) A method of providing ordered data [to a device] transmitted from a data source to a data destination over a bus [with a weakly ordered interface], [the bus providing a communication path for data and associated addresses,] comprising the steps of:

writing items of data into sequentially ordered areas of a memory [to form a sequence of items of data], the items of data having a predefined order in the data source, the sequentially ordered areas of memory being identifiable by addresses, each item of data being placed in an area having an associated address in the data source;

transmitting the items of data and [the] associated addresses from the data source to the data destination over the bus, the items of data being transmitted in an order other than the predefined order;

receiving the items of data and the associated addresses in the data source from the bus;

examining the associated address in the data source for each item of data received from the bus; and

placing each item of data received from the bus in one of multiple sequentially arranged areas of a storing buffer, each item being placed based on the associated address [of] in the data source for each item, the placement of the items of data [forming the sequence of items] causing reordering of the received items of data.

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14. (reinstated and once amended) A method of increasing effective bus bandwidth for transmitting items of data from a data source to a data destination, comprising the steps of:

defining a region of a memory as a write combining memory type, the region of the memory being comprised of addressable locations of processor memory, the addressable locations identifiable by [an address] addresses in the data source;

writing items of data into the region in a sequential order of the addressable locations, the items of data comprising encoded commands and parameters associated with the encoded commands, [with the number of parameters associated with the command and the meaning of parameters in the sequential order indicated by the encoded commands] the items of data having a predefined order in the data source;

[providing] transmitting the items of data and addresses of the items of data from the data source to the data destination over a bus [to a coprocessor], the items of data being transmitted in an order other than the predefined order; and

arranging the transmitted items of data in an order corresponding to the [sequential order of addressable locations upon receipt] addresses in the data source for [of] the items of data [by the coprocessor] to reorder the transmitted items of data.

15. (reinstated and once amended) The method of increasing effective bus bandwidth of claim 14 further comprising the steps of determining which items of data in the order corresponding to the sequential order of addressable locations are encoded commands and further determining which parameters are associated with each encoded command and the meaning of the parameters based on their position in the order of addressable locations.

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16. (once amended) A bus interface unit of a computer device, the bus interface unit being coupled to a bus with a weakly ordered interface providing information comprised of data items and associated addresses received from a data source, the bus interface unit comprising:

a plurality of storage buffers each having a plurality of slots for storing data items, the plurality of slots being identifiable by addresses in the data source;

a first router for routing the data items received from the bus to a particular one of the plurality of storage buffers based on a first part of the [address] addresses in the data source associated with the data [item] items; and

a plurality of second routers for each of the storage buffers for routing the data items routed to [a] the particular one of the storage buffers to one of the slots in the particular one of the storage buffers based on a second part of the [address] addresses in the data source associated with the data [item] items.

23. (once amended) A computer device for reordering incoming data received from a data source over a bus interface, the incoming data having a predefined order and associated address information in the data source, comprising:

a receive buffer which receives the incoming data and the associated address information in the data source, the received incoming data being out of the predefined order;

a storage buffer which stores the incoming data in an order based on the associated address information in the data source; and

a detector which determines proper placement of the out order incoming data in the receive buffer in the storage buffer based on the associated address information in the data source.

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30. (once amended) A method of reordering incoming data transmitted from a data source to a data destination, the incoming data containing address information in the data source, the incoming data being in a predefined order in the data source and being transmitted from the data source to the data destination in an order other than the predefined order, the method comprising the steps of:

receiving at the data destination the incoming data and the address information transmitted from the data source;

arranging, in the predefined order, the incoming data based on the address information in the data source contained within the incoming data; and

storing the arranged data temporarily.

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